

An Efficient Implementation of Acute Lymphoblastic Leukemia Images Segmentation on the FPGA

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ABSTRACT

In the medical field, image segmentation process is considered the most essential step in image analysis. In this work, the color segmentation for acute lymphoblastic leukemia images (ALL) is applied to segment each leukemia image into two clearly defined regions: blasts and background. The ALL segmentation process is based on hue channel (H) of HSV color space as a method in segmentation of WBC from its complicated background. This work presents an efficient framework for segmentation of ALL images on a reconfigurable logic platform using Simulink, MATLAB and Xilinx System Generator (XSG). This segmentation framework is implemented on a FPGA using basic Xilinx Blockset to minimize hardware resources and lower execution time to be suitable enough for medical applications. It is designed using XSG as DSP design tool that enables the use of Simulink models, implemented in VHDL and synthesized for three different Xilinx FPGA boards.

Keywords: Color segmentation, FPGA, ALL, XSG.

1 Introduction

The term Leukemia refers to a group of cancers resulting from abnormal increase of the white blood cells (WBCs) that divided and grew in uncontrolled way. These WBCs start from the bone marrow and shift quickly into the blood to reach to other parts of the body such as spleen, lymph nodes and liver. Thus, early diagnosis and treatment applied to these WBCs are vital.

Leukemia can be categorized into: acute and chronic. Acute leukemia spreads very quickly and has to be treated immediately rather than chronic leukemia where immediate treatment is not a must. Also, acute leukemia can be either lymphoblastic (ALL) or myelogenous (AML), based on affected cell type. Chronic leukemia can be either lymphoblastic (CLL) or myelogenous (CML) [1]. Acute lymphoblastic leukemia (ALL) is considered to be the main focus of this work because the survival rate is expected to be higher when other types.

According to image processing field, segmentation process is considered the most demanding tasks. It is used to partitioning a digital image into a number of different meaningful regions. For biomedical imaging applications, image segmentation is a founding step in image analysis [2] as it will directly affect the post-processing. It is a crucial component in diagnosis [3] [4] and treatment [5].

The main aim of acute leukemia blood cell segmentation is to extract component such as WBCs from its complicated background. There are many techniques that have been developed for image segmentation [6] [7] [8]. Due to the complex nature of blood cells and overlapping between these cells, segmenting them remains a challenging task [9]. Many algorithms for segmentation have been developed for color images that produce more information of the scene than grayscale images do [10]. For leukemia segmentation process, transformations of original RGB images to different color spaces such as (HSI, HSV, YUV, XYZ, Lab...etc.) are proposed in many works. According to [11], Lab color space is used for segmentation process. Also, algorithm based on HSI color space is proposed in [12]. Based on HSV color space, segmentation technique [13] for ALL images is proposed.

Image processing algorithms implemented in FPGA have emerged as the most viable solution for improving the performance of image processing systems. It offers a compromise between the flexibility of general purpose processors and ASICs. FPGAs are recently used in many image processing applications such as image compression [14] [15] [16] [17], image filtering [18] [19] and wireless communication [20] [21] [22]. Xilinx System Generator is a DSP design tool [23] [24] that deal with many images processing application. XSG is a part of the ISE design suite that provides Xilinx DSP Blockset for application specific design. The main advantage of using Xilinx system generator for FPGA implementation is that Xilinx blockset provides close integration with MATLAB Simulink that helps in co-simulating the FPGA module with pixel vector provided by MATLAB Simulink Blocks [25].

This work focuses on implementing multilevel thresholding segmentation technique efficiently based on color histogram of H channel of HSV color space on FPGA using basic Xilinx blockset. Firstly, all algorithms are implemented in MATLAB to realize the segmentation results. The pipelined framework of multilevel thresholding image segmentation is implemented on three FPGA devices Spartan3E xc3s500e-4fg320, Spartan 3A DSP 3400A-4fg676 and Spartan 3AN xc3s700an-5fgg484.

2 Proposed Framework

A typical acute lymphoblastic leukemia sample consists of three main regions: abnormal white blood cells (blast), red blood cell (RBC) and background areas. Nucleus and cytoplasm regions formed a blast and contain important information to be observed by hematologists. However, the RBC and background regions contain no information and can be eliminated from the image. In this work, the proposed framework is divided into two main parts. The first part is to apply the color image segmentation technique on ALL images using HSV color space. For the second part, this segmentation technique is implemented on FPGA using basic Xilinx blockset. The proposed framework involves the following steps:

2.1 Image Database

Microscope Images of ALL are taken from ALL-IDB database [26]. An optical laboratory microscope together with a Canon Power Shot G5 camera was used to capture the images of the database. In addition, all images are in JPG format with 24 bit color depth, resolution 2592×1944 . Moreover, the images are taken with different magnifications of the microscope ranging from 300 to 500. ALL-IDB2 version of the database is used as well. Figure 1 shows the sample of ALL images.

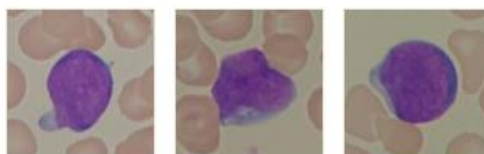


Figure 1: Sample of ALL images

2.2 Acute Lymphoblastic Leukemia Segmentation

According to the inherent interdependence between luminance and chrominance in the RGB color space, a HSV color space is used. HSV provides useful chromatic information of the image that located in a single channel without any luminance effect. Also, HSV color space is familiar to human perception and more suitable for image processing than RGB color space [27]. HSV color space contains three channels. The hue (H) channel refers to the color type such as (Red, Green, Yellow...etc.). The range of hue values changes from 0° to 360° passing through rainbow colors. Saturation (S) value affects the purity of the colors while Value (V) means the amount of light in the color. Both S and V range from 0 to 1. H channel that only needed for ALL segmentation process is obtained by transforming the source image from RGB color space to HSV color space based on the following equations:

$$H = \begin{cases} 0 & \text{if } M = m \\ \left(60^\circ \times \frac{g - b}{M - m} + 0^\circ\right) \bmod 360^\circ & \text{if } M = r \\ 60^\circ \times \frac{b - r}{M - m} + 120^\circ & \text{if } M = g \\ 60^\circ \times \frac{r - g}{M - m} + 240^\circ & \text{if } M = b \end{cases}$$

Where:

M means the maximum values in *R*, *G*, and *B* elements.

m means the minimum values in *R*, *G*, and *B* elements.

To segment ALL images into blasts and background using H channel of HSV color space. There are 6 steps involved in applying image segmentation process as shown in figure 2.

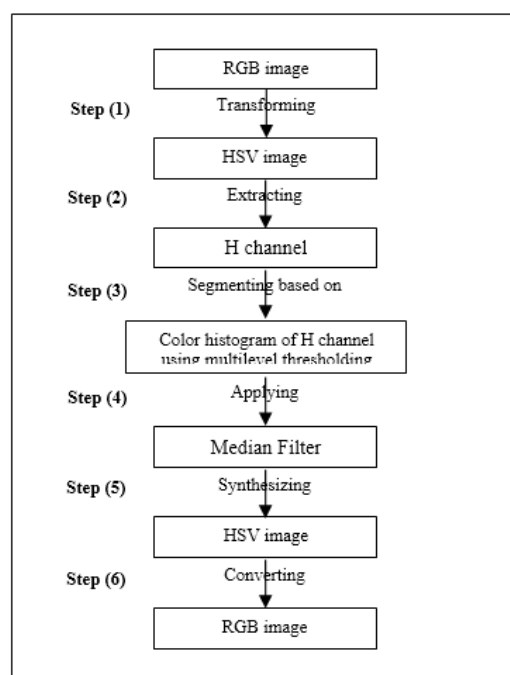


Figure 2: Block diagram of ALL segmentation using HSV

2.3 FPGA Implementation

Although computers keep getting faster and faster, there are always new image processing applications that need more processing than is available. Field Programmable Gate Arrays are very capable devices in the area of digital signal processing. They are semiconductor devices that contain a number of logic blocks, which can be programmed to perform complex image processing algorithms. The main purpose of this work is to implement color image segmentation technique on a FPGA more efficient than [28] by using only basic Xilinx blockset. Segmentation based on FPGA is designed using XSG that enables the use of Simulink models and implemented using VHDL.

Due to the implementation process based on FPGA, the pre-processing and post-processing steps for ALL segmentation are proposed using Simulink blocks. Figure 3 presents color space conversion block from RGB to HSV image and applying median filter to H channel for further processing.

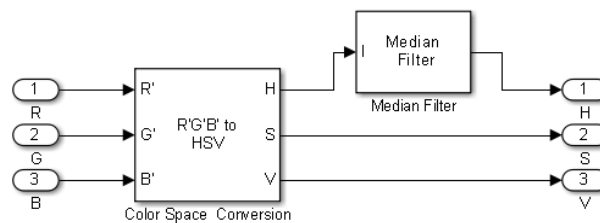


Figure 3: Pre-processing for ALL segmentation

To accomplishing Image processing task using Xilinx System Generator, two Software tools are needed to be installed. This work uses MATLAB version R2012b and Xilinx ISE 14.5. The model is built for image segmentation using library provided by Xilinx Blockset. According to the design of segmentation to meet FPGA requirements, pre-processing the HSV image prior to the main FPGA framework is needed due to the nature of FPGA that deals with an image as a vector. Also, image post-processing is required. There are three stages involved in ALL FPGA segmentation process using Simulink and Xilinx blocks:

- FPGA pre-processing
- Xilinx models for FPGA segmentation
- FPGA post-processing

Figure 4 represents the main block diagram of FPGA segmentation framework.

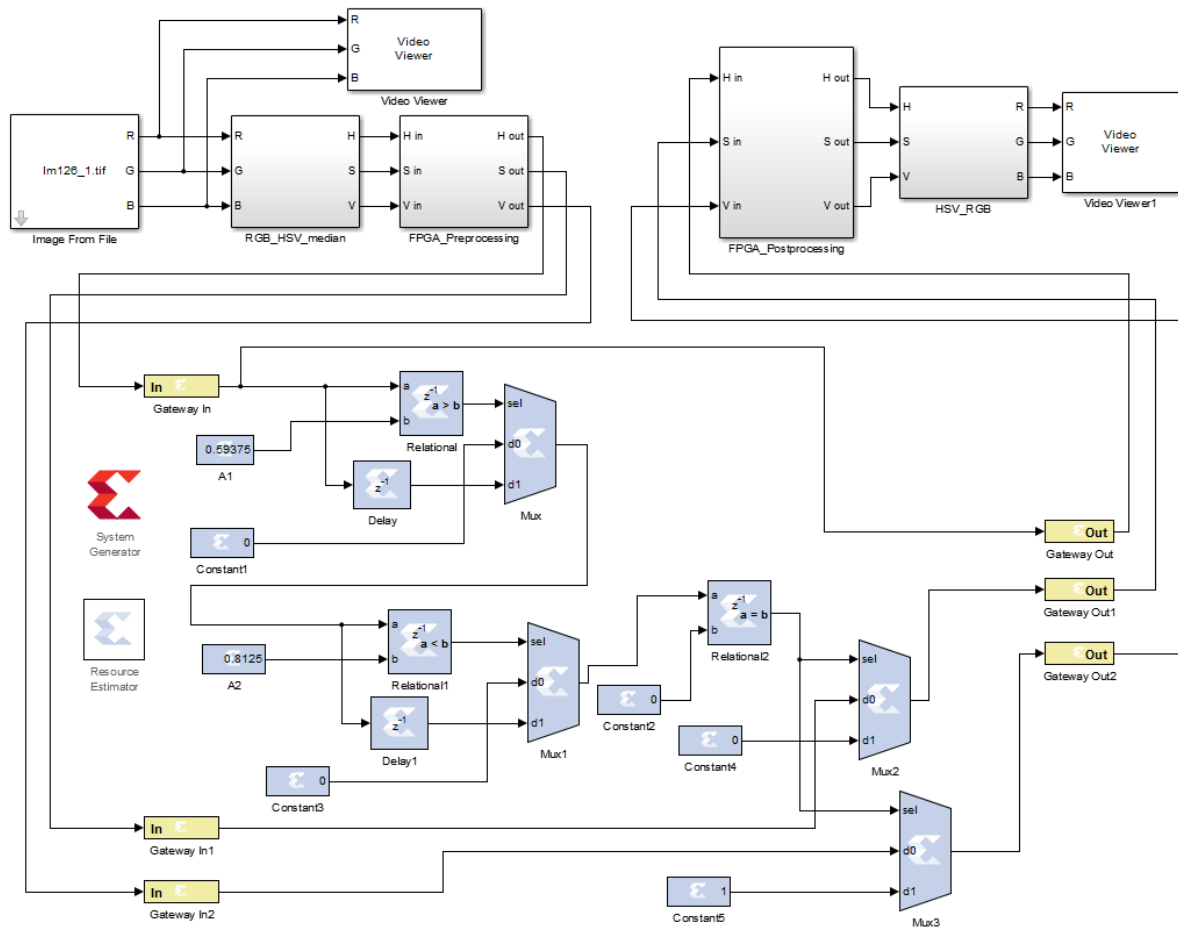


Figure 4: Block diagram of proposed framework

The image pixels are provided to Xilinx models in the form of multidimensional H|S|V separate color signals in the form of vector in Xilinx fixed point format. The reflected results can be seen on a video viewer. Once the expected results are obtained, XSG is configured to be suitable for SPARTAN-3E Starter kit xc3S500e-fg320, SPARTAN 3A DSP 3400A-4fg676 and SPARTAN 3AN xc3s700an-5fgg484 FPGAs.

2.3.1 FPGA Pre-Processing

Pre-processing blocks provide an input image suitable for FPGA as vector array. Reshape blocks convert the HSV image channels into single array of pixels. The process of setting sampling mode is obtained using frame conversion. Unbuffer blocks convert this frame to scalar samples output at a higher sampling rate. The model based design used for image pre-processing for FPGA is shown in Figure 5.

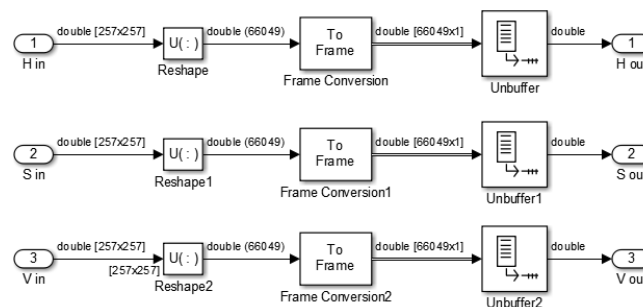


Figure 5: FPGA Pre-processing

2.3.2 Xilinx Models for FPGA Segmentation

FPGA segmentation process is modeled using Xilinx blocks. Once the FPGA boundaries have been established using the Gateway In and Gateway Out blocks, the DSP design can be constructed using Xilinx DSP blocks. Within the Gateway In and Gateway Out blocks, Simulink blocks are not supported for use.

Xilinx fixed point type conversion is made by Gateway In blocks. Image Segmentation process is achieved based on two angle values that obtained from color histogram of H channel. These two values are represented using two constant blocks. Multilevel thresholding operated using Relational and Mux blocks. This is followed by certain blocks to merge all the processed data. Figure 6 shows the ALL segmentation using basic Xilinx blocks while figure 7 presents ghost image using basic Xilinx blocks.

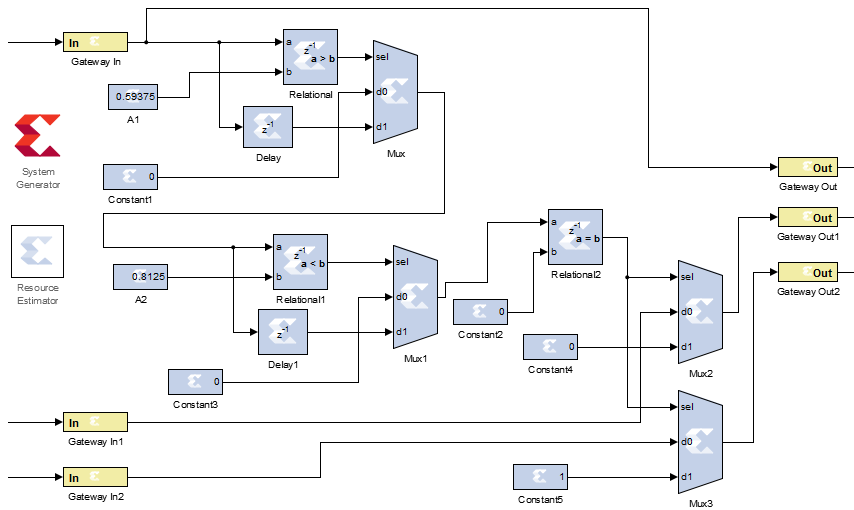


Figure 6: Segmentation of ALL images using standard Xilinx blocks

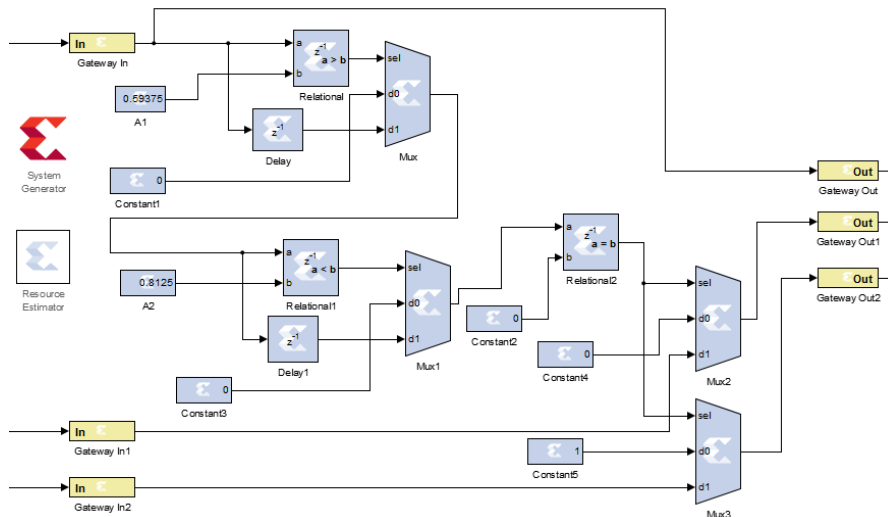


Figure 7: Ghost image for ALL using standard Xilinx blocks

2.3.3 FPGA Post-Processing

Post-processing blocks converts an image from vector to 2D matrix as shown in figure 8. Buffer blocks are used to convert scalar samples to frame output at lower sampling rate. The process of converting 1D image to 2D image is obtained using reshape blocks.

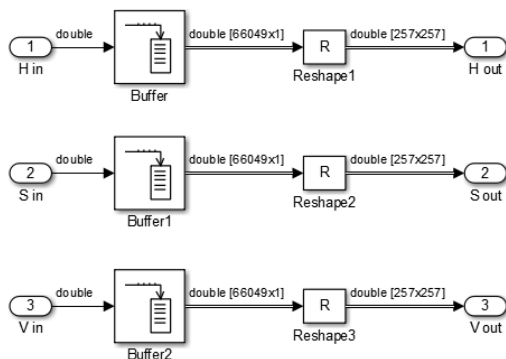


Figure 8: FPGA Post-processing

2.4 FPGA Co-Simulation

Once the results are obtained from FPGA design; the model is implemented for JTAG FPGA co-simulation. The system generator parameters are set and generated. On compilation, programming file in VHDL is created to be accessed by Xilinx ISE. The module is synthesized and implemented on FPGA. Figure 9 illustrates the FPGA co-simulation block.

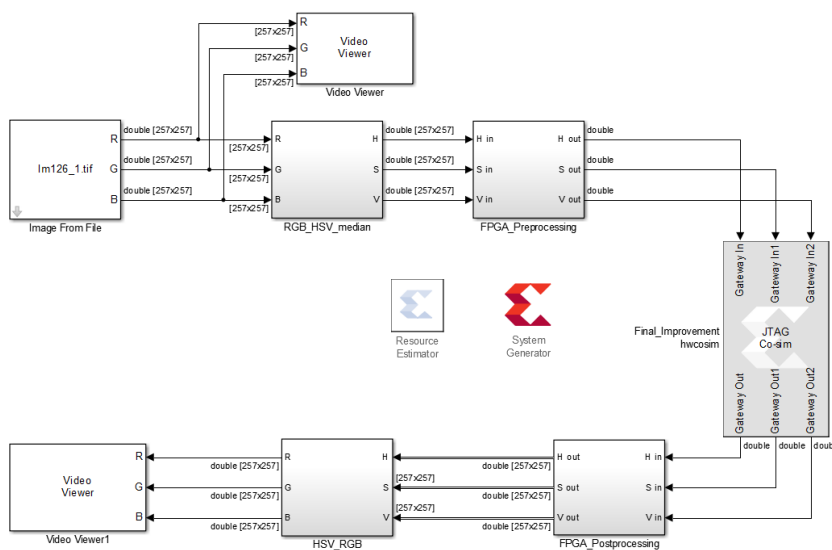


Figure 9: FPGA co-simulation

3 Results and Discussion

The segmentation framework based HSV color space described above is tested on two blood samples of ALL. The results obtained after applying proposed framework are shown in figure 10:

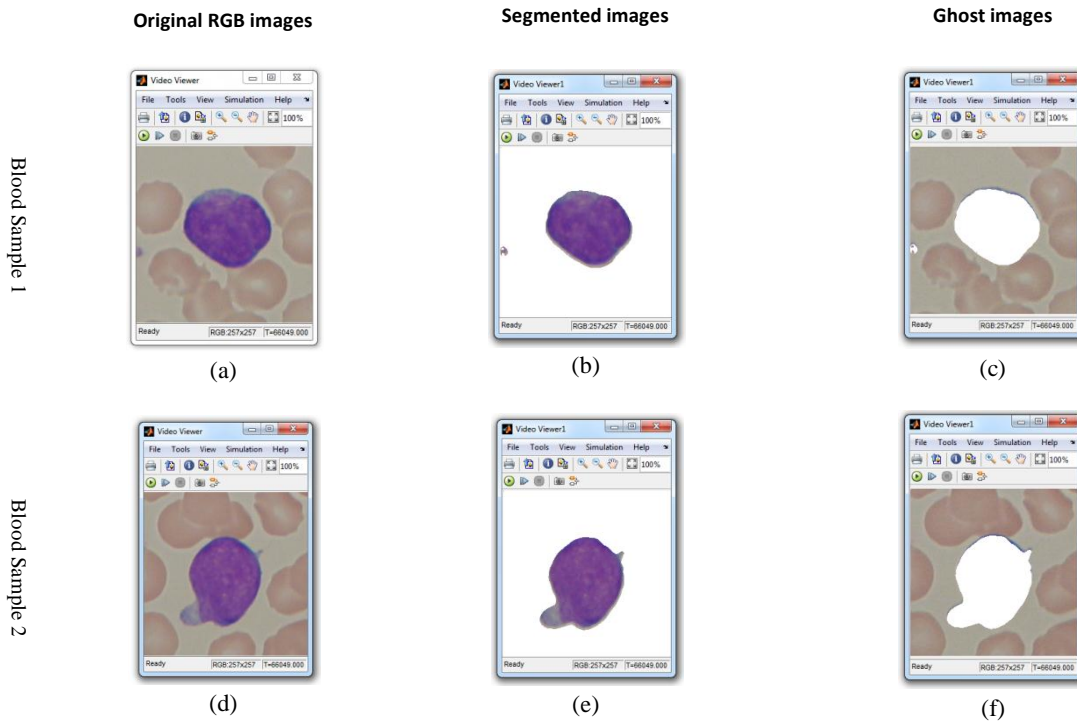


Figure 10: Segmentation of ALL Based HSV Color Space

Figure 10 (a) and figure 10 (d) represent the original RGB acute leukemia images. Meanwhile, figure 10 (b) and figure 10 (e) shows the output images after blasts segmentation process. Finally, Figure 10 (c) and figure 10 (f) show the ghost images for segmented images.

For FPGA implementation process, SPARTAN-3E Starter kit xc3S500e-fg320, SPARTAN 3A DSP 3400A-4fg676 and SPARTAN 3AN xc3s700an-5fgg484 resource usage is estimated for proposed framework as shown in table 1. The VHDL code for the proposed FPGA segmentation has 2381 lines of VHDL code. This is due to the huge amount of floating point-fixed point conversions.

Table 1: FPGA resources used in the implementation for ALL segmentation

	Spartan3E xc3s500e-4fg320		Spartan 3A DSP 3400A-4fg676		Spartan 3AN xc3s700an-5fgg484	
	Used	Available	Used	Available	Used	Available
Number of Slices Flip Flop	23	9312	23	47744	23	11776
Number of Occupied Slice	30	4656	27	23872	34	5888
Number of 4 input LUTs	40	9312	40	47744	40	11776
Number of Bonded IOBs	61	232	61	469	61	372
Maximum Frequency	291.72 MHz		310.17 MHz		366.845 MHz	

4 Conclusion

In this work, a performance comparison using image segmentation framework that applied on three FPGA devices for ALL blast detection is performed. The improved segmentation framework that implemented on FPGA is designed using only basic Xilinx Blockset. The design of FPGA segmentation framework implemented on SPARTAN 3AN xc3s700an-5fgg484 achieves 2.726 ns at 366.85 MHz as best minimum period. The design framework used in this work can be used for all Xilinx FPGA Kits. In the future work, the result of this work can be used as the basis for features extraction from the acute lymphoblastic leukemia blood samples.

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