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A Logic Circuit Simulation for Choosing a Group or a Question using Register and Encoder

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ABSTRACT

Besides learning and working individually, normally people also interact in a group. A teacher or manager will divide and put several persons in groups, and mostly the group arrangement will be organized according to some classifications. This is quite different when people are dealing with a specific game or quiz. The participants will be asked to choose their own group or question in random order. Using the basic concept of digital system and electronic workbench 5.12 software, a logic circuit could be designed to build a circuit simulation consists of register and encoder which can be used to choose a group or a question randomly. The methods being used are study literature, analysis, design, and simulation. The result shows a desired output, a logic circuit for choosing a group or a question can be built using register and encoder logic components. Once a group or a question has been chosen, it cannot be chosen and displayed again.

Keywords: Choosing a Group; Choosing a Question; Logic Circuit Simulation; Register; Decoder.

1 Introduction

People sometimes do social interactions in daily works or learning. Generally the most fun interactions are quiz and game. When people are dealing with a specific game or quiz, they will be asked to choose their own group or question in a random order. Developing the basic concept of digital system we have learned and applying electronic workbench 5.12 software, we can try to build a simple and fun logic circuit simulation consists of main components: register and encoder, which can be used to choose a group or a question randomly. Once a group or a question has been chosen, it cannot be chosen and displayed again.

2 Methods

Learning from several methodologies from [8], the methodology being used for this research mainly to understand the basic concept and combine the functions of shift register and encoder, to derive a new and simple form of designing a counter.

3 Basic Theories

3.1 Synchronous Counter

Synchronous Counter is a type of sequential logic circuit functions for counting binary information, which clock input of all the flip-flop components are connected together and triggered by the input pulses. Thus, all the flip-flops would change state simultaneously, in parallel [1,2,6,7]. The number of

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bit depends on number of flip-flop being used. For example, in Figure 1, to have a design output values in 3-bit length, the number of flip-flop that we used is 3 (three) also. The bit-sequences are given in Table 1.

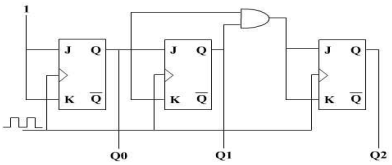


Figure 1. 3-bit synchronous counter

Table 1. The bit sequence of 3-bit synchronous counter

FF2	FF1	FF0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

3.2 Shift Register

Shift register is another type of sequential logic circuit, mainly for storing digital data. They are a group of flip-flops, usually D-FF, connected in a loop so that the output from one flip-flop becomes the input of the next flip-flop, and so on [1,2,5]. All the flip-flops are driven by a common clock, and all are set or reset simultaneously. This is shown in Figure 2.

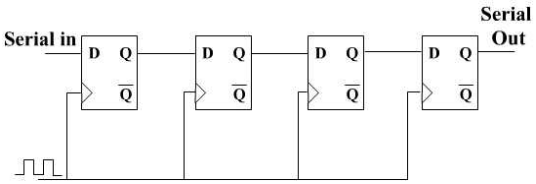


Figure 2. Right shift register

3.3 Encoder

Encoder is a type of combinational logic circuit, mostly used in data encoding. The design for encoder comes from logic gate circuits. It has an input of 2^nlines and output n lines as being referred in [1,2,3,4].

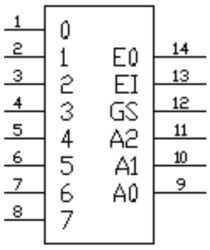


Figure 3. Encoder 8-to-3

A simple form of low-active encoder is shown in Figure 3. The outputs will activate a binary number combination based on the active input and priority. To understand how a priority encoder works, there is a characteristic table being given in Table 2. If logic 1 is given to more than one input of priority encoder, the output will read the highest input level, and transfer it as a combination of output.

Table 2. Tuth table of a priority encoder

INPUTS				OUTPUTS	
D0	D1	D2	D3	A	B
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1
x	1	0	0	0	1
x	x	1	0	1	0
x	x	x	1	1	1

4 Analysis and Design

4.1 Analysis

A right shift register has a very simple form like the circuit diagram in Figure 2. It functions a serial input. The binary input will come from the left side, and shifted to the right. Every clock cycle will shift one bit to the right. We can add as many flip-flops as we need, according to our design, as explained in [2,3,5]. What will happen if we try to modify the right shift register circuit by adding an XNOR gate? With this circuit connection, the LED light will light one by one each cycle: 100, 010, 001, 100, … etc. The related logic circuit is shown in Figure 4.

Table 3. Tuth table of an xnor gate

INPUTS		OUTPUT
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

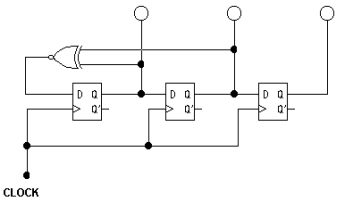


Figure 4. Right shift register with an xnor gate

At an initial condition, the outputs of all Flip-flops are 0s and will turn into 1s if the inputs are 1s. From the circuit we can see that Q_1=0 and Q_2=0, being an input for XNOR Gate. The output of Xnor gate will give logic 1, so input D will become 1. The next clock cycle will set the output of Q_1=1, and followed by Q_2=1 again in the next cyle. When Q_1 was changing into 1s, Xnor gate will give an output of 0s, turn D

into 0s once again. The next cycle will give an output of Q_1=0, and so on. These happen continuously and build a same loop of function.

4.2 Design

In my research, the output of right shift register is connected as an input for encoder to build a synchronous counter 1-3, as shown in figure 5.

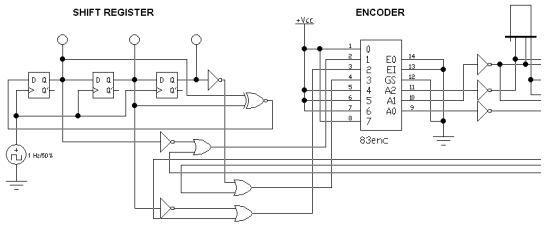
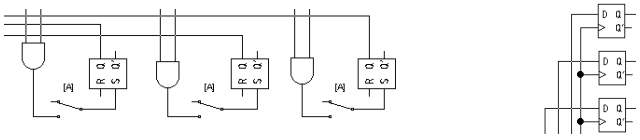


Figure 5. Synchronous counter with shift register and encoder

Each output of D FFs is connected to the correspond number in encoder. The output will display 1 to 3 continuously.

To choose a group or number, we must use a switch. Once a group or a question has been chosen, it cannot be chosen and displayed again, so we will need a component to lock the number being chosen so it will not display again in the counter output. In here an R-S latch has been used for that function, and a D latch is used to display the picked up group or question.



(a) (b)

Figure 6. (a) Switch and (b) D-latch

5 Simulation

Now we can try to connect all the logic parts and integrate them together to build the logic circuit for a quiz or a game. From the simulations using software Electronic Workbench 5.12, the circuit works well and gives the right output. The synchronous counter displays a number between 1 to 3. A participant needs to push the button switch to pick up a group or question from the counter. When the switch already selects the number, the counter will start to count again without the number already chosen or displayed. Now it is the next participant turn to push the button switch and select from the rest of numbers. In this simulation, I used a 1 Hz clock in order to be able to follow the counter display.

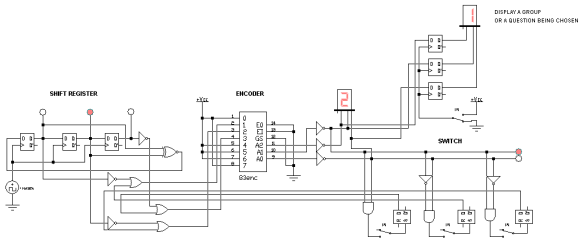


Figure 7. First Simulation shows that group/question 1 is being chosen from loop counter (1 to 3)

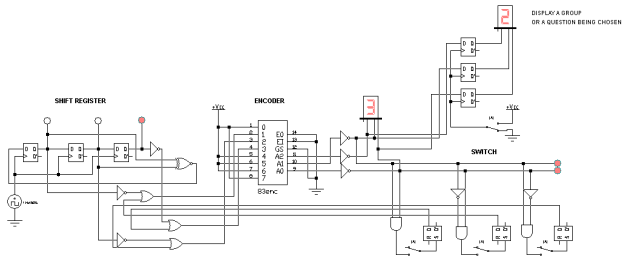


Figure 8. Second Simulation shows that group/question 2 is being chosen from loop counter (2 and 3)

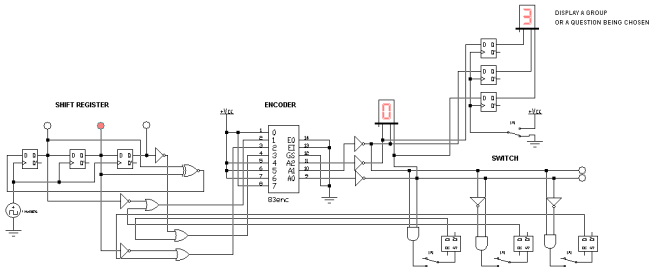


Figure 9. Third Simulation shows that the only option left is being chosen: group/question 3

6 Conclusion

Using Register and Encoder, we can build a logic circuit simulation for choosing a group or a question. Uniquely, once a group or a question being selected by a participant, it cannot be selected or displayed anymore by other participants. That is why it will be fun to use this simulation for a game or a quiz. The logic circuit simulation only used a low frequency clock so we could see the changes shown by the counter. It must be upgraded into a high frequency clock so participants cannot see the numbers and randomly can select one of them. For this purpose, a simple modification shall be made to synchronize the counter and the button. Hopefully this research outcome will be useful for learning digital system in the future.

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